

**Amendment and Response**

Applicant: Irwin Aberin et al.

Serial No.: 10/588,927

Filed: August 3, 2007

Docket No.: I431.168.101/FIN581PCT/US

Title: SEMICONDUCTOR PACKAGE WITH PERFORATED SUBSTRATE

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**REMARKS**

The following remarks are made in response to the Non-Final Office Action mailed May 7, 2009. Claims 1-16 have been previously cancelled without prejudice. Claims 17-36 were rejected. Claim 25 was objected to. With this Response, claims 17, 22-25, 30, 32, and 33 have been amended. Claims 17-36 remain pending in the application and are presented for reconsideration and allowance.

**Claim Objections**

Claim 25 was objected to for an informality.

With this Response, claim 25 has been amended so as to correct the identified informality. As such, Applicants respectfully request that the rejection to claim 25 be withdrawn.

**Claim Rejections under 35 U.S.C. § 112**

Claim 33 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With the Response, the means language has been removed from claim 33. As such, Applicants respectfully request that the rejection of claim 33 under 35 U.S.C. 112, second paragraph, be withdrawn.

**Claim Rejections under 35 U.S.C. § 103**

Claims 17-21 and 24-36 were rejected under 35 U.S.C. 103(a) as being obvious over Okada in view of US 6,054,755 A to Takamichi et al. (hereinafter "Takamichi").

Claim 22 was rejected under 35 U.S.C. 103(a) as being obvious over Okada in view of Takamichi, and further in view of US Patent Pub. No. 2002/0043721 A1 to Weber (hereinafter "Weber").

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Applicants respectfully submit that neither Okada nor Takamichi, either alone or in combination, teach or suggest the semiconductor package as defined by independent claim 30. Okada teaches forming vent holes 16 through regions of an organic substrate 6 which are below where a semiconductor chip 2 is to be mounted so as to provide a pathway to release moisture from the organic substrate which would otherwise be trapped by an adhesive 4 used to fix the semiconductor chip 2 to the organic substrate, with such trapped moisture otherwise creating damaging inner pressure when the substrate is heated during mounting of the semiconductor chip to the substrate (Figure 1, paragraphs 0007 to 0009].

There is no teaching or suggestion whatsoever in Okada that vent holes should be provided anywhere other than directly below the semiconductor chip. As described by the present specification, such “adjacent vent holes” provide venting of water from the substrate in areas other than directly below the semiconductor which also become heated so as to thereby further reduce internal stresses during manufacturing (e.g., during a solder reflow process), as described by the present specification (page 3, lines 4-9) Providing vent holes in locations other than directly below the semiconductor chip is also advantageous if the semiconductor chip is over-molded or over-encapsulated as moisture from the molding material can escape through such adjacent vent holes, as also described by the present specification (page 4, lines 19-26).

Takamichi was cited only to teach that vent holes may be closed at one end with a layer of solder resist, and also fails to teach or suggest providing vent holes at locations other than directly below a semiconductor chip mounting location.

In light of the above, Applicants respectfully submit that neither Okada nor Takamichi, either alone or in combination, teach or suggest **a plurality of non-plated vent holes which are distributed in the substrate so as to be below and adjacent to the semiconductor chip**, as defined by amended independent claim 30. There is simply no teaching or suggest whatsoever in either Okada or Takamichi as to the benefits to be gained by providing vent holes in locations other than directly below the semiconductor chip. As such, one of ordinary skill in the art would not have modified the cited references to position vent holes anywhere but under the semiconductor chip as such a person would have no expectation of the advantageous technical

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effects of such a modified arrangement. As such, Applicants respectfully request that the rejection of independent claim 30 under 35 U.S.C. 103 be withdrawn and that independent claim 30 be allowed.

Independent claims 17, 22, 24, and 33 have each been amended to include limitations similar to those described above with respect to independent claim 30. As such, for at least the reasons remarked upon above with respect to independent claim 30, Applicants respectfully request that the rejections of independent claims 17, 22, 24, and 33 under 35 U.S.C. 103(a) also be withdrawn and that independent claims 17, 22, 24, and 33 be allowed as well.

Claims 18-21 further define patentably distinct independent claim 17, claims 25-29 further define patentably distinct independent claim 24, claims 31 and 32 further define patentably distinct independent claim 30, and claims 34-36 further define patentably distinct independent claim 33. As such, Applicants respectfully request that the rejections of dependent claims 18-21, 25-29, 31, 32, and 34-36 under 35 U.S.C. 103(a) also be withdrawn and that dependent claims 18-21, 25-29, 31, 32, and 34-36 be allowed as well.

**Claim Rejections under 35 U.S.C. § 102**

Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Pub. No. 2001/0042908 A1 to Okada et al. (hereinafter "Okada").

With this Response, claim 23 has been amended so as to depend from independent claim 22. As described above, Applicants believe independent claim 22 to be in form for allowance over the art of record. As such, Applicants submit that claim 22 is also in form for allowance over the art of record.

Accordingly, Applicants respectfully request that the rejection of claims 23 under 35 U.S.C. 102 be withdrawn and that claim 23 be allowed.

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**CONCLUSION**

In view of the above, Applicant respectfully submits that pending claims 17-36 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 17-36 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Steven E. Dicke at Telephone No. (612) 573-2002, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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